U.G. 2nd Semester Examination - 2022

BCA

[HONOURS]

Course Code : BBCACCHC201

Course Title: Digital Logic

Full Marks : 30 Time : 2 Hours

The figures in the right-hand margin indicate marks.

Candidates are required to give their answers in their own words as far as practicable.

1. Answer any **ten** questions: 1×10=10

a) Define maxterm and minterm.

b) $(11001010.1101)_2 = (?)_H$.

c) What do you mean by universal gate? Give one example.

d) State distributive law.

e) Write the advantage of using don't care in K-Map.

f) Differentiate between sequential and combinational circuit.

g) Write the truth table of R-s flip-flop.

h) Demonstrate DeMorgan's theorem.

i) What do you mean by race condition?

j) What do you mean by trigger?

k) What is 'ripple counter'?

l) What is shift register?

m) Find the 10's complement of $(314)_{10}$.

n) Draw the diagram for serial-in-serial-out (SISO) register.

o) Show that EX-OR is complement of EX-NOR.

2. Answer any **five** questions: 2×5=10

a) Simplify the following expression using K-Map:

$F(A, B, C, D) = \Sigma_m (8, 10, 11, 12, 13, 14, 15)$

b) Simplify the boolean expression:

$$Y = \overline{\overline{A\bar{B} + ABC} + A\left(B + A\bar{B}\right)}$$

c) Design T flip-flop using JK flip-flop.

d) Draw Full-subtractor circuit using only half-subtractors.

e) Design :

i) One OR gate using only NAND gates and ii) One AND gate using only NOR gates.

f) State the differences between ecoder and decoder.

g) Subtract 57 from 24 using 2's complementary method.

h) Design full adder using Decoder and external OR gate.

3. Answer any **two** questions: 5×2=10

a) i) Design a counter with the following binary sequence: 0, 4, 2, 1, 6 using J-K flip-flop.

ii) Explain the operation of universal shift register. 2+3

b) i) Define Register.

ii) Design a mod-8 counter using JK flip-flop. 1+4

c) Design a 8 to 1 multiplexer by using the four variable function given by F(A, B, C, D) = Σ_m (0, 1, 3, 4, 8, 9, 15). 5

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