## **U.G. 4th Semester Examination - 2022**

## **BCA**

## [HONOURS]

**Course Code: BBCASEHT 405** 

**Course Title: Computer Organization** 

Full Marks: 50 Time: 2 Hours

The figures in the right-hand margin indicate marks.

Answer **all** the following questions by choosing the correct alternative out of four options:  $2 \times 25 = 50$ 

- 1. Which type of memory cannot be directly accessed by the CPU?
  - a) Primary Memory
  - b) Cache Memory
  - c) Secondary Memory
  - d) Registers
- 2. Which Cache mapping technique is also known as Many-to-Many Mapping?
  - a) Direct Mapping
  - b) Associative Mapping
  - c) Set-Associative Mapping
  - d) None of the above

- 3. Which of the following is/are the ways of implementing Hardwired Control Unit?
  - a) State Table Method
  - b) Delay Element Method
  - c) Sequence Counter Method
  - d) All of the above
- 4. Match the following:

<b>List-I (Addressing Modes)</b>	List-II (Implementation)
A. Indirect Addressing Mode	I. Loops
B. Immediate	II. Pointers
C. Auto-Increment	III. Constants

- a) A-II, B-III, C-I
- b) A-II, B-I, C-III
- c) A-I, B-III, C-II
- d) A-III, B-I, C-II
- 5. Which Addressing Mode is suitable for passing array as parameter?
  - a) Indirect Addressing Mode
  - b) Indexed Addressing Mode
  - c) Relative Addressing Mode
  - d) Implied Addressing Mode

6. XCHG, MOV, PUSH and POP are examples of which			10.	The full form of RISC is:		
types of instruction?				a)	Reduced Instruction Set Computer	
a)	Data Manipulation Instruction	ns		b)	Random Instruction Set Computer	
b)	Data Transfer Instructions			c)	Register Instruction Set Computer	
c)	Program Control Instructions	S		d)	Register Input Sequence Counter	
d)	Logical Instructions		11.	Zero	Address instruction are commonly found in	
7. Wilkes Design is used to implement—				which type of CPU organisation?		
a)	Parallel Computers			a)	Single Accumulator Organisation	
b)	Hardwired Control Unit			b)	General Register Organisation	
c)	Micro Programmed Control	Unit		c)	Stack Organisation	
d)	Multi Programming Control		12.	d)	None of the above	
,					der a cache with 128 blocks of 16-words each.	
a)					J generates 16 bit address. What is the tag size if	
b)	Secondary Memory			a)	ay set associative mapping is used?  6 bits	
	Control Memory			a) b)	7 bits	
c)	•			c)	8 bits	
d)	Nano Memory			d)	9 bits	
9. Which of the following is not a property of Static			13.		ich of the following register keeps track of the	
	<ul><li>RAM?</li><li>a) They are used to implement Cache Memory</li></ul>			instructions stored in the program stored in		
a)		Cache Memory		memory?		
b)	Refresh Circuit is needed	1 MOGERTI		a)	Accumulator	
c)	Made up of Flip-flops and MOSFET's		b)	Address Register		
d)	(transistors) Consumes more power			c)	Program Counter	
				d)	Index Register	
461/BCA	(3)	[Turn Over]	461/I	BCA	(4)	

14.	_	roup of bits that tell the cor		18.	The	e disadvantage/s of the hardwired approach is	
	spec	specific operation is known as—				·	
	a)	Instruction code			a)	It is less flexible	
	b)	Micro-operation			b)	It cannot be used for complex instructions	
	c)	Accumulator			c)	It is costly	
	d)	Register			d)	Less flexible and cannot be used for complex	
15.	Which bus is used to connect the various parts in order to provide a direct connection to CPU—				instructions		
			19.	Wha	at is the formula for Hit Ratio?		
	a)	Processor inter-connectiv	ity bus		a)	Hit/(Hit + Miss)	
	b)	Processor bus Memory bus			b)	Miss/(Hit + Miss)	
	c)				c)	(Hit + Miss) / Miss	
	d)	Control bus	rol bus		d)	(Hit + Miss) / Hit	
16.	The	b) Returning c) Process execution		20.	Indi	ividual control words of the micro routine are	
	of tl				called—		
	a)				<ul><li>a)</li><li>b)</li><li>c)</li><li>d)</li></ul>	Micro task	
	b)					Micro operation	
	c)					Micro instruction	
	d)					Micro command	
17.	Who	When an instruction is read from the memory, it is called—  a) Memory Read cycle  b) Fetch cycle  c) Instruction cycle		21.		read the control words sequentially is used.	
	call					Program counter	
	a)						
	b)				b) c)	Instruction register	
	c)					Micro program counter	
	d) Memory write cycle			d)	None of the above		
461/1	BCA	(5)	[Turn Over]	461/	BCA	(6)	

- 22. Advantages of Pipelining are
  - a) The cycle time of the processor is reduced
  - b) It increases the throughput of the system
  - c) It makes the system reliable
  - d) All of the above
- 23. EPROM is used for
  - a) Erasing the data of ROM
  - b) Reconstructing data of ROM
  - c) Duplicating ROM
  - d) Erasing and reconstructing data of ROM
- 24. The technique that extends storage capacities of the main memory beyond the actual size of the main memory is known as
  - a) Multitasking
  - b) Multiprocessing
  - c) Virtual storage
  - d) Multiprogramming
- 25. How is the effective address of base-register calculated?
  - a) By addition of index register contents to the partial address in instruction

- b) By addition of implied register contents to the partial address in instruction
- c) By addition of index register contents to the complete address in instruction
- d) By addition of implied register contents to the complete address in instruction